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FORM PTO-1390 (REV 9-2001) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY 'S DOCKET NUMBER: 97-GR2-144

U S APPLICATION NO (If known, see 37 CFR 1 5): 10/070080

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR00/02367	(24.08.00) 24 August 2000	(02.09.99) 02 September 1999

TITLE OF INVENTION
METHOD FOR PACKAGING A SEMICONDUCTOR CHIP CONTAINING SENSORS AND RESULTING PACKAGE

APPLICANT(S) FOR DO/EO/US
Antonio DO BENTO VIEIRA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [x] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [x] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [x] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [x] has been communicated by the International Bureau.
   c [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [ ] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [ ] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau)
   b. [ ] have been communicated by the International Bureau.
   c [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16 [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U S.C. 154(d)(4)
20. [x] Other items or information:
    Copy of Form PCT/IB/308

US APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/070080	PCT/FR00/02367	97-GR2-144

21. ☒ The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	- 20 =		x **$18.00**	$	
Independent claims	- 3 =		x **$84.00**	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$	

TOTAL OF ABOVE CALCULATIONS =	$ 1,020.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2. +	$	
SUBTOTAL =	$ 1,020.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).	$ 130.00	
TOTAL NATIONAL FEE =	$	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$	
TOTAL FEES ENCLOSED =	$ 1,150.00	
Amount to be refunded:	$	
charged:	$	

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 50-1556 in the amount of $ 1,150.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-1556 . A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

FLEIT, KAIN, GIBBONS,
GUTMAN & BONGINI P.L.
551 N.W. 77TH STREET
SUITE 111
BOCA RATON, FLORIDA 33487

Jose Gutman
SIGNATURE

Jose Gutman
NAME

35,171
REGISTRATION NUMBER

EXPRESS MAIL LABEL NO. EL863782124US
DATE MAILED: July 1, 2002

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Atty. Docket: 97-GR2-144
Antonio DO BENTO VIEIRA	:	Examiner: Unknown
Application No. 10/070,080	:	Group Art Unit: Unknown
I.A. Filing Date: August 24, 2000	:	

For: METHOD FOR PACKAGING A SEMICONDUCTOR CHIP CONTAINING SENSORS AND RESULTING PACKAGE

CERTIFICATE OF EXPRESS MAIL DELIVERY

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS EXPRESS MAIL IN AN ENVELOPE ADDRESSED TO:
COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, D.C. 20231, ON: 7/1/02
Date of Deposit

Kathleen Smith
Name of Person Depositing Correspondence With USPS

Kathleen Smith 7/1/02
SIGNATURE DATE

PRELIMINARY AMENDMENT UNDER 37 C.F.R. § 1.115

Commissioner for Patents
Washington, D.C. 20231

SIR:

Please enter and consider the following amendment and remarks prior to examination of the above-identified application.

IN THE ABSTRACT - (CLEAN COPY)

Please delete the Abstract section without prejudice, and replace it with the following.

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ABSTRACT

A method for producing a package (30) for a semiconductor die (or chip) including a semiconductor die (20) having one or more bond pads on the top surface for providing terminals for one or more sensors (22) in the upper surface and a die carrier (32) including an opening (34) and one or more external terminals. The semiconductor die (20) upper surface is fixed to the die carrier (32) and each bond pad is coupled to a portion of the external terminals exposed at the die carrier (32) lower surface, for example, with weld points (42). A sealing ring (44,46) encapsulates the interface zone (40) and a coating material (48) encapsulates the die carrier (32) lower surface and a lower surface of the semiconductor die (20).

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IN THE CLAIMS - (CLEAN COPY)

Please cancel claims 1-19 without prejudice.

Please add new Claims 20-46, as follows.

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20. (New) A method for packaging a semiconductor die, the method comprising the steps of:

attaching a surface of a semiconductor die to a surface of a die carrier having external lead bonds or terminals, such that this die carrier does not extend in front of one or more sensors provided on the top surface of the semiconductor die and one or more bond pads on the top surface of the semiconductor die are coupled to one or more of the bond pads of said die carrier in an annular interface area formed between the top surface of the semiconductor die and a surface of said die carrier;

encapsulating said interface area with a sealing ring; and

encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material.

21. (New) The method according to claim 20, further comprising the steps of:

attaching a top surface of the semiconductor die to a bottom surface of the die carrier such that one or more sensors within the top surface of the semiconductor die are disposed below a first opening in the die carrier that is larger than the one or more sensors but smaller than the semiconductor die, and an interface area is formed between said die and said die carrier where the top surface of the semiconductor die extends beyond the first opening in the die carrier and one or more bond pads on the top surface of the semiconductor die are coupled to one or more of the exterior terminals on the bottom surface of the die carrier;

curing the semiconductor die attached to the die carrier;

encapsulating the interface area with a sealing ring;

curing the sealing ring;

encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material; and

curing the packaging material.

22. (New) The method according to claim 21, further comprising the steps of:

encapsulating an exterior portion of the interface area with a first sealing ring;

curing the first sealing ring;

encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material;

curing the packaging material;

encapsulating an interior portion of the interface area with a second sealing ring; and

curing the second sealing ring.

23. (New) The method according to claim 20, further comprising the steps of:

attaching a bottom surface of a semiconductor die to a top surface of a recessed area of a pre-printed frame, the recessed area being larger than the semiconductor die, the semiconductor die having one or more bond pads on a top surface for providing terminals to one or more sensors within the top surface, and the pre-printed frame having one or more wire leads;

curing the semiconductor die attached to the pre-printed frame;

forming a dam to surround the recessed area to prevent a packaging material from entering the recessed area;

curing the dam;

forming wire bonds to couple each bond pad to a portion of one of the wire leads that is near the recessed area;

encapsulating the wire bonds with a sealing ring;

curing the sealing material;

encapsulating the bottom surface of the pre-printed frame with the packaging material; and

curing the packaging material.

24. (New) The method according to claim 20, further comprising the step of applying a protective coating over the one or more sensors of the semiconductor.

25. (New) The method according to claim 20, further comprising:

attaching a cap having a second opening larger than the sensors of the semiconductor die, the cap being attached to the top surface of the die carrier; and

substantially encapsulating the cap with the packaging material.

26. (New) The method according to claim 20, further comprising:

installing at least one of a lens and a filter in or above a first opening in the die carrier.

27. (New) The method according to claim 20, further comprising:

installing at least one of a lens and a filter above one or more sensors within the top surface of the semiconductor die.

28. (New) A semiconductor die package, comprising:

a semiconductor die having one or more bond pads on a top surface for providing terminals to one or more sensors, in particular optical sensors, within the top surface;

a die carrier which does not extend in front of said sensors and which has one or more bond pads comprising bond terminals and having external lead bonds, the bond pads of said die carrier and the bond pads of said die determining between them an annular interface area and being coupled in this area;

a sealing ring encapsulating said interface area; and

a packaging material encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die.

29. (New) The semiconductor die package according to claim 28, wherein the die carrier has a pre-printed frame and each external terminal comprises a wire lead.

30. (New) The semiconductor die package according to claim 29, further comprising:

a cap having a second opening similar in size to the first opening, the cap being attached to the top surface of the pre-printed wire frame and the packaging material substantially encapsulating said cap.

31. (New) The semiconductor die package according to claim 30, wherein the cap is attached to the pre-printed frame by a polymide adhesive.

32. (New) The semiconductor die package according to claim 28, wherein the die

carrier has a first opening larger than the one or more sensors but smaller than the semiconductor die and has one or more external terminals, the top surface of the semiconductor die being attached to the bottom surface of the die carrier such that the one or more sensors are disposed below the first opening and an interface area is formed where the top surface of the semiconductor die extends beyond the first opening in the die carrier and each bond pad is coupled to a portion of one of the external terminals that is exposed on the bottom surface of the die carrier, and the semiconductor die package further comprising:

a sealing ring encapsulating the interface area; and

a packaging material encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die.

33. (New) The semiconductor die package according to claim 32, wherein the sealing ring comprises a first external sealing ring and a second internal sealing ring.

34. (New) The semiconductor die package according to claim 32, wherein said sealing ring and/or said packaging material comprise a thixotropic epoxy-based material.

35. (New) The semiconductor die package according to claim 32, wherein each bond pad is coupled to one of the external pads on the bottom surface of the die carrier by a solder bump.

36. (New) The semiconductor die package according to claim 32, wherein the die carrier comprises a substrate and each external terminal comprises a bond pad formed on a top surface of the substrate.

37. (New) The semiconductor die package according to claim 32, wherein the one or more sensors are covered with a protective layer.

38. (New) The semiconductor die package according to claim 32, further comprising:

a transparent encapsulation material in the first opening and on the top surface of the semiconductor die.

39. (New) The semiconductor die package according to claim 32, further comprising:

a lens disposed above the one or more sensors.

40. (New) The semiconductor die package according to claim 28, further comprising:

a pre-printed frame having a recessed area which is larger than the semiconductor die and having one or more wire leads, a bottom surface of the semiconductor die being attached to a top surface of the recessed area of the pre-printed frame;

a wire bond coupling each bond pad to a portion of one of the external terminals near the recessed area;

a dam surrounding the recessed area to prevent packaging material from entering the recessed area;

a sealing material encapsulating each wire bond; and

a package material encapsulating the bottom surface of the pre-printed frame.

41. (New) The semiconductor die package according to claim 40, further comprising:

a cap having a second opening similar in size to the first opening, the cap being attached to the top surface of the pre-printed wire frame and the packaging material substantially encapsulating said cap.

42. (New) The semiconductor die package according to claim 42, wherein the cap is attached to the pre-printed frame by a polymide adhesive.

43. (New) The semiconductor die package according to claim 40, wherein said sealing ring and/or said packaging material comprise a thixotropic epoxy-based material.

44. (New) The semiconductor die package according to claim 40, wherein the one or more sensors are covered with a protective layer.

45. (New) The semiconductor die package according to claim 40, further comprising:

a transparent encapsulation material in the first opening and on the top surface of the semiconductor die.

46. (New) The semiconductor die package according to claim 40, further comprising:

a lens disposed above the one or more sensors.

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REMARKS

By virtue of this amendment, claims 20-46 are pending in the application. Claims 1-19 have been canceled without prejudice. New claims 20-46 have been added. An examination of this application is respectfully requested in light of this preliminary amendment and the following remarks.

This preliminary amendment has been filed to place the claims in better form for examination. Claims 20-46 have been substituted for original claims 1-19. An action on the merits is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

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The present application, after entry of this amendment, comprises twenty-seven (27) claims, including two (2) independent claims. Applicant has paid the basic filing fee for twenty (20) claims including three (3) independent claims. Applicant, therefore, believes that an additional fee of **$126** (=7 * $18) is currently due.

The Commissioner is hereby authorized to charge the additional fee of **$126**, and further authorized to charge any fees which may be required or credit any overpayment to Deposit Account **50-1556**.

Applicant believes that the claims as amended are in condition for allowance. Examination and consideration of the application, as amended, are requested.

Respectfully submitted,

Date: July 1, 2002 By: _____

Jose Gutman
Reg. No. 35,171

Please send all correspondence concerning this patent application to:

Jose Gutman, Esq.

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Method for packaging a semiconductor die containing sensors and package obtained

The present invention relates generally to packaging semiconductor dies and more particularly to a method for packaging a semiconductor die containing one or more sensors and to a package resulting in particular from this method.

Without limiting the scope of the present invention, the background of the present invention is described in connection with the packaging of semiconductor dies containing one or more optical sensors, which can be any sensors designed to detect any spectrum of light, including infrared. Accordingly, the present invention is applicable to the packaging of any semiconductor die containing one or more sensors, such as fingerprint sensors, where conventional packaging techniques and materials reduce the effectiveness of the sensors.

Semiconductor dies or integrated circuits containing optical sensors, unlike most semiconductor dies, must be packaged in such a way as to allow light to contact the optical sensors and motion sensors, but still protect these sensors from environmental contamination. This is also true for infrared sensors, such as those used in integrated circuit fingerprint sensors. As a result, the performance and sensitivity of optical and other sensors can be significantly diminished by contaminants and moisture introduced during the packaging process, or by contaminants, air bubbles, irregularities and deformities in the packaging material itself.

In addition, some packages for semiconductor dies containing sensors utilize a transparent plastic resin or epoxy resin.

The use of a transparent plastic resin or epoxy

resin, however, introduces additional problems. First, the most commonly used agents to facilitate the molding of the package and increase the package's reliability cannot be used. Second, these transparent materials are harder to handle and clean out of the molds. Third, these materials are more expensive and require lengthy cure times (2 to 3 times that of a normal package).

Accordingly, there is a need for a method for packaging semiconductor dies containing one or more sensors that is durable, economical, efficient and effective. More specifically, the package should not significantly interfere with sensor performance while simultaneously protecting the sensors from foreign materials and contaminants.

The subject of the present invention is first of all a method for packaging a semiconductor die which comprises the steps of attaching a surface of a semiconductor die to a surface of a die carrier having external lead bonds or terminals, such that this die carrier does not extend in front of one or more sensors provided on the top surface of the semiconductor die and one or more bond pads on the top surface of the semiconductor die are coupled to one or more of the bond pads of said die carrier in an annular interface area formed between the top surface of the semiconductor die and a surface of said die carrier; encapsulating said interface area with a sealing ring; and encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material.

According to an alternative embodiment of the invention, the method comprises the steps of: attaching a top surface of a semiconductor die to a bottom surface of a die carrier such that one or more sensors within the top surface of the semiconductor die are disposed below a first opening in the die carrier that is larger than the

one or more sensors but smaller than the semiconductor die and an interface area is formed between said die and said die carrier where the top surface of the semiconductor die extends beyond the first opening in the die carrier and one or more bond pads on the top surface of the semiconductor die are coupled to one or more of the exterior terminals on the bottom surface of the die carrier; curing the semiconductor die attached to the die carrier; encapsulating the interface area with a sealing ring; curing the sealing ring; encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material; and curing the packaging material.

According to the invention, the method may advantageously comprise the steps of: encapsulating an exterior portion of the interface area with a first sealing ring; curing the first sealing ring; encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material; curing the packaging material; encapsulating an interior portion of the interface area with a second sealing ring; and curing the second sealing ring.

According to another alternative embodiment of the invention, the method comprises the steps of: attaching a bottom surface of a semiconductor die to a top surface of a recessed area of a pre-printed frame, the recessed area being larger than the semiconductor die, the semiconductor die having one or more bond pads on a top surface for providing terminals to one or more sensors within the top surface, and the pre-printed frame having one or more wire leads; curing the semiconductor die attached to the pre-printed frame; forming a dam to surround the recessed area to prevent a packaging material from entering the recessed area; curing the dam; forming wire bonds to couple each bond pad to a portion

of one of the wire leads that is near the recessed area; encapsulating the wire bonds with a sealing ring; curing the sealing material; encapsulating the bottom surface of the pre-printed frame with the packaging material; and curing the packaging material.

According to the invention, the method may advantageously further comprise a step of applying a protective coating over the one or more sensors of the semiconductor die.

According to the invention, the method may advantageously furthermore comprise attaching a cap having a second opening larger than the sensors of the semiconductor die, the cap being attached to the top surface of the die carrier; and substantially encapsulating the cap with the packaging material.

Another subject of the invention is a semiconductor die package comprising a semiconductor die having one or more bond pads on a top surface for providing terminals to one or more sensors, in particular optical sensors, within the top surface; a die carrier which does not extend in front of said sensors and which has one or more bond pads comprising bond terminals and having external lead bonds, the bond pads of said die carrier and the bond pads of said die determining between them an annular interface area and being coupled in this area; a sealing ring encapsulating said interface area; and a packaging material encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die.

According to the invention, the package may advantageously comprise a die carrier having a first opening larger than the one or more sensors but smaller than the semiconductor die and one or more external terminals; the top surface of the semiconductor die attached to the bottom surface of the die carrier such that the one or more sensors are disposed below the first

opening and an interface area is formed where the top surface of the semiconductor die extends beyond the first opening in the die carrier and each bond pad is coupled to a portion of one of the external terminals that is exposed on the bottom surface of the die carrier; a sealing ring encapsulating the interface area; and a packaging material encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die.

According to the invention, the sealing ring may advantageously comprise a first external sealing ring and a second internal sealing ring.

According to the invention, each bond pad is coupled to one of the external pads on the bottom surface of the die carrier by a solder bump.

According to the invention, the die carrier may advantageously comprise a substrate and each external terminal comprises a bond pad formed on a top surface of the substrate.

According to the invention, the die carrier may advantageously comprise a pre-printed frame and each external terminal comprises a wire lead.

According to the invention, the package may advantageously comprise a pre-printed frame having a recessed area which is larger than the semiconductor die and one or more wire leads, a bottom surface of the semiconductor die being attached to a top surface of the recessed area of the pre-printed frame; a wire bond coupling each bond pad to a portion of one of the external terminals near the recessed area; a dam surrounding the recessed area to prevent packaging material from entering the recessed area; a sealing material encapsulating each wire bond; and a package material encapsulating the bottom surface of the pre-printed frame.

According to the invention, the package may advantageously furthermore comprise a cap having a second opening similar in size to the first opening, the cap being attached to the top surface of the pre-printed wire frame and the packaging material substantially encapsulating said cap.

According to the invention, said sealing ring and/or said packaging material may advantageously comprise a thixotropic epoxy-based material.

According to the invention, the one or more sensors are covered with a protective layer.

According to the invention, the package may advantageously furthermore comprise a transparent encapsulation material in the first opening and on the top surface of the semiconductor die.

According to the invention, the package may advantageously furthermore comprise a lens disposed above the one or more sensors.

The above and further advantages of the invention may be better understood by referring to the following description in conjunction with the appended drawings, in which:

Figures 1A-1C depict a top view of a semiconductor die having one or more sensors in accordance with the present invention;

Figure 2 depicts a top view of a package for a semiconductor die having one or more sensors in accordance with a first embodiment of the present invention;

Figure 3 depicts a cross sectional view of the package depicted in Figure 2 in accordance with the first embodiment of the present invention;

Figures 4A-4D depict, in cross sectional views, the method of producing the package depicted in Figures 2 and 3 in accordance with the first embodiment of the present

invention;

Figures 5A-5F depict, in cross sectional views, the method of producing a package for a semiconductor die having one or more sensors in accordance with a second embodiment of the present invention; and

Figures 6A-6F depict, in cross sectional views, the method of producing a package for a semiconductor die having one or more sensors in accordance with a third embodiment of the present invention.

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and do not limit the scope of the invention.

The descriptions of the figures to follow discuss methods of packaging semiconductor dies containing sensors whose functionality and reliability depend on the fundamental characteristics of light traveling to or from the device. In addition, the packaging methods described below are equally applicable to other types of sensors, such as fingerprint sensors. The discussion centers around general flip chip or wire bonded attachments, but is not intended to limit the scope of the invention to these configurations, since the method of packaging may be used for any chip attachment configuration. Moreover, lenses and other focusing or filtering elements can be easily added to the packages described below.

Turning now to Figure 1A, a top view of a semiconductor die 20 having a quad bond pad row arrangement is depicted and will now be described. The semiconductor die 20 has a sensor area 22, which contains one or more sensors (not shown), and one or more bond

pads 24. The one or more sensors (not shown) are typically optical sensors or sensors designed to detect any spectrum of light, including infrared. The one or more sensors (not shown) may also be fingerprint sensors or some other type of non-optical sensor. The sensor area 22, however, may also contain additional circuitry (not shown), such as control, memory, processing or other non-sensing circuits. The bond pads 24 are located between the sensor area 22 and the perimeter of the semiconductor die 20, and provide terminals to the one or more sensors (not shown) contained in the sensor area 22. The bond pads 24 may be arranged in a quad bond pad row arrangement (Figure 1A), dual bond pad row arrangement 26 (Figure 1B), or a single bond pad row arrangement 28 (Figure 1C). In any case, the number and configuration of the bond pads 24 on the semiconductor die 20 may vary and are not limited by Figures 1A, 1B and 1C.

Now referring to Figure 2, a top view of a package for a semiconductor die containing one or more sensors in accordance with a first embodiment of the present invention is denoted generally as 30 and will now be described. The package 30 comprises a semiconductor die 20 attached to a die carrier or substrate 32. The semiconductor die 20 has one or more bond pads 24 on the top surface in a quad bond pad row arrangement. As previously mentioned in reference to Figures 1A, 1B and 1C, the number and configuration of the bond pads 24 can vary. The substrate 32 has an opening 34, which is larger than the sensor area 22, but smaller than the semiconductor die 20 and the one or more bond pads 24. The opening 34 extends all the way through the substrate 32.

The top surface of the semiconductor die 20 is attached to the bottom surface of the substrate 32 so that the sensor area 22 is disposed below the opening 34

and an interface area 40 (Figure 3) is formed where the top surface of the semiconductor die 20 extends beyond the opening 34 in the substrate 32 and each bond pad 24 is coupled to one of the external terminals 36 with a solder bump 42 (Figure 3).

Now referring to Figure 3, a cross-sectional view of the package depicted in Figure 2 is shown. As previously described, the package 30 comprises a semiconductor die 20 attached to a substrate 32. The semiconductor die 20 has a sensor area 22, which is preferably covered with a protective layer 38. The substrate 32 has an opening 34, which is larger than the sensor area 22, but smaller than the semiconductor die 20 and the one or more bond pads 24 (Figure 2). The opening 34 extends all the way through the substrate 32.

The top surface of the semiconductor die 20 is attached to the bottom surface of the substrate 32 so that the sensor area 22 is disposed below the opening 34 and an annular interface area 40 is formed where the top surface of the semiconductor die 20 extends beyond the opening 34 in the substrate 32 and each bond pad 24 is coupled to one of the external terminals 36 with a solder bump 42. The external terminals 36 are strategically placed over the top surface of the substrate 32 to provide a physical connection to the bond pads 24 once the solder bumps 42 are re-flowed.

The interface area 40 is encapsulated with a sealing ring, which may be applied in a two stage process to form a first sealing ring 44 and a second sealing ring 46. The single sealing ring configuration may be used when the solder bumps 42 can be encapsulated while maintaining the required thermal cycle/shock performance, such as in low cost situations where lower reliability is acceptable. The two sealing ring configuration, however, provides increased reliability. The first sealing ring 44

provides good mechanical definition of the exposed sensor area 22 that results in mechanical accuracy, repeatability and reproducibility. The second sealing ring 46 provides higher reliability in terms of thermal cycle/shock performance and prevents failure mechanisms caused by cracked solder bumps 42 due to excessive stress induced by differences in the thermal coefficient of expansion of the first sealing ring 44, packaging material 48, and the substrate 32. Either way, the sealing rings 44 and 46 prevent any packaging material 48 from getting into the sensor area 22.

The first sealing ring 44 encapsulates the exterior portion of the interface area 40, whereas the second sealing ring 46 encapsulates the interior portion of the interface area 40. The first sealing ring 44 preferably comprises a high-purity, thixotropic epoxy-based non-flowing retaining dam material having a high glass transition temperature with a low coefficient of thermal expansion and an excellent thermal shock/cycle performance. The second sealing ring 46 preferably comprises a high-purity, high-flow underfilling material having a low coefficient of thermal expansion and an excellent thermal shock/cycle performance. If only one sealing ring is used, it should comprise a high-purity, thixotropic epoxy-based non-flowing retaining dam material having a high glass transition temperature with a low coefficient of thermal expansion and an excellent thermal shock/cycle performance.

The bottom surface of the substrate 32 and the bottom surface of the semiconductor die 20 are encapsulated with a packaging material 48. The packaging material 48 preferably comprises a high-purity, thixotropic epoxy-based encapsulant material having a low coefficient of thermal expansion and an excellent thermal shock/cycle performance.

Now referring to Figures 4A-4D, the method of manufacturing the package depicted in Figures 2 and 3 will be described. As will be readily appreciated by those skilled in the art, some of the steps described below may be modified or combined into a single step to produce an equivalent device. Accordingly, the present invention is not strictly limited by the order described or depicted in the following figures.

Step one (Figure 4A): The top surface of the semiconductor die 20 is attached to the bottom surface of the die carrier or substrate 32 such that the sensor area 22 containing the one or more sensors within the top surface of the semiconductor die 20 is disposed below the opening 34 in the substrate 32. The opening 34 is larger than the sensor area 22, but is smaller than the semiconductor die 20. An annular interface area 40 (Figure 3) is formed where the top surface of the semiconductor die 20 extends beyond the opening 34 in the substrate 32. Each bond pad 24 (Figure 2) is coupled to one of the external terminals 36 (Figure 2) that are exposed on the bottom surface of the substrate 32 with a solder bump 42. The assembly (substrate 32 and semiconductor die 20) is then cured.

Step two (Figure 4B): The exterior portion 50 of the interface area 40 (Figure 3) is encapsulated with the first sealing ring 44. The first sealing ring is then cured.

Step three (Figure 4C): The bottom surface of the substrate 32 and the bottom surface of the semiconductor die 20 are encapsulated with a packaging material 48. The packaging material 48 is then cured.

Step four (Figure 4D): The interior portion 52 of the interface area 40 (Figure 3) is encapsulated with a second sealing ring 46. The second sealing ring is then cured. Note that the first and second sealing rings 44

and 46 can be combined into a single sealing ring that encapsulates the interface area 40 (Figure 3), thus eliminating step four.

Step five (Figure 3): The protective layer 38 is formed on top of the sensor area 22 and the external terminals 36 are formed. A lens or filter may also be installed in or above the opening 34 (Figures 2 and 4A). The package is then preferably cleaned.

Now referring to Figures 5A-5F, the method of manufacturing a package in accordance with a second embodiment of the present invention will be described. In this embodiment, a pre-printed frame 60 is used as the die carrier, rather than the substrate 32 in Figures 2-4D. Pre-printed frames 60 are well known by those skilled in the art and typically contain one or more etched and stamped wire leads (not shown) and frame alignment holes (not shown).

Step one (Figure 5A): The top surface of the semiconductor die 20 is attached to the bottom surface of the die carrier or pre-printed frame 60 such that the sensor area 22 containing the one or more sensors within the top surface of the semiconductor die 20 is disposed below the first opening 34 in the pre-printed frame 60. The first opening 34 is larger than the sensor area 22, but is smaller than the semiconductor die 20. An annular interface area 66 (Figure 5D) is formed where the top surface of the semiconductor die 20 extends beyond the opening 34 in the preprinted frame 60. Each bond pad 24 (Figures 1A, 1B or 1C) is coupled to one of the external terminals or wire leads 74 (Figure 5F) that are exposed on the bottom surface of the pre-printed frame 60 with a solder bump 42. The assembly (pre-printed frame 60 and semiconductor die 20) is then cured.

Step two (Figure 5B): The exterior portion 62 of the interface area 66 (Figure 5D) is encapsulated with

the first sealing ring 44. The first sealing ring is then cured.

Step three (Figure 5C): The interior portion 64 of the interface area 66 (Figure 5D) is encapsulated with a second sealing ring 46. The second sealing ring is then cured. Note that the first and second sealing rings 44 and 46 can be combined into a single sealing ring that encapsulates the interface area 66 (Figure 5D), thus eliminating step three.

Step four (Figure 5D): A cap 68 is attached to the top surface of the pre-printed frame 60 with an adhesive 70, such as a polymide adhesive. The cap 68 has a second opening 72 similar in size to the first opening 34 in the pre-printed frame 60. The cap 68 adds mechanical strength and stability to the package. The assembly is then cured.

Step five (Figure 5E): The bottom surface of the pre-printed frame 60 and the bottom surface of the semiconductor die 20 are encapsulated and the cap 68 is substantially encapsulated with a packaging material 48. The packaging material 48 is then cured.

Step six (Figure 5E): The protective layer 38 is formed on top of the sensor area 22 and the external terminals or wire leads 74 are trimmed and formed. A lens or filter may also be installed in or above the first opening 34 or second opening 72 (Figure 5D). The package is then preferably cured.

Now referring to Figures 6A-6F, the method of manufacturing a package in accordance with a third embodiment of the present invention will be described. In this embodiment, like Figures 5A-5F, a pre-printed frame 80 is used as the die carrier. This pre-printed frame 80, however, does not have a first opening 34 (Figure 5D). Instead, the pre-printed frame 80 has a recessed area 82 that is larger than the semiconductor die 20. This arrangement provides a low-profile package.

Step one (Figure 6A): The bottom surface of the semiconductor die 20 is attached to the top surface of the recessed area 82 of the pre-printed frame 80 with an adhesive 84, such as a polymide adhesive. The assembly (pre-printed frame 80 and semiconductor die 20) is then cured.

Steps two and three (Figure 6B): A dam 86 is formed to surround the recessed area 82 and prevent the packaging material 48 (Figure 6E) from entering the recessed area 82 and the semiconductor die 20. The dam is then cured. Wire bonds 88 are formed to couple each bond pad 24 (Figures 1A, 1B and 1C) to a portion of one of the wire leads 98 (Figure 6F) that is near the recessed area 82. Wire bonding is well known to those skilled in the art.

Step four (Figure 6C): A cap 90 is attached to the top surface of the pre-printed frame 80 with an adhesive 84, such as a polymide adhesive. The cap 90 has an opening 92 above the portion of each of the exterior terminals 94 that is near the recessed area 82, the dam 86 surrounding the recessed area 82, and the recessed area 82. The cap 68 adds mechanical strength and stability to the package. The assembly is then cured.

Step five (Figure 6D): The wire bonds 88 are encapsulated with a sealing material 96. The sealing material 96 is then cured.

Step six (Figure 6E): The bottom surface of the pre-printed frame 80, the dam 86 and the recessed area 82 are encapsulated and the cap 90 is substantially encapsulated with a packaging material 48. The packaging material 48 is then cured.

Step six (Figure 6F): The protective layer 38 is formed on top of the sensor area 22 and the external terminals or wire leads 98 are trimmed and formed. A lens or filter may also be installed in or above the opening

92 (Figure 6C). The package is then preferably cleaned.

Although preferred embodiments of the invention have been described in detail, it will be understood by those skilled in the art that various modifications can be made therein without departing from the spirit and scope of the invention as set forth in the appended claims.

CLAIMS

1. Method for packaging a semiconductor die characterized in that it comprises the steps of:

attaching a surface of a semiconductor die (20) to a surface of a die carrier (32) having external lead bonds or terminals (36, 74), such that this die carrier does not extend in front of one or more sensors (22) provided on the top surface of the semiconductor die and one or more bond pads (24) on the top surface of the semiconductor die are coupled to one or more of the bond pads of said die carrier in an annular interface area (40) formed between the top surface of the semiconductor die and a surface of said die carrier;

encapsulating said interface area (40) with a sealing ring (44, 96); and

encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material (48).

2. Method according to claim 1 characterized in that it comprises the steps of:

attaching a top surface of a semiconductor die (20) to a bottom surface of a die carrier (32) such that one or more sensors within the top surface of the semiconductor die are disposed below a first opening (34) in the die carrier that is larger than the one or more sensors but smaller than the semiconductor die and an interface area (40) is formed between said die and said die carrier where the top surface of the semiconductor die extends beyond the first opening in the die carrier and one or more bond pads on the top surface of the semiconductor die are coupled to one or more of the exterior terminals on the bottom surface of the die carrier;

curing the semiconductor die attached to the die carrier;

encapsulating the interface area (40) with a sealing ring (44);

curing the sealing ring;

encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material (48); and

curing the packaging material.

3. Method according to claim 2 characterized in that it comprises the steps of:

encapsulating an exterior portion of the interface area with a first sealing ring (44);

curing the first sealing ring;

encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die with a packaging material (48);

curing the packaging material;

encapsulating an interior portion of the interface area with a second sealing ring (46); and

curing the second sealing ring.

4. Method according to claim 1 characterized in that it comprises the steps of:

attaching a bottom surface of a semiconductor die (20) to a top surface of a recessed area (82) of a pre-printed frame, the recessed area being larger than the semiconductor die, the semiconductor die having one or more bond pads on a top surface for providing terminals to one or more sensors within the top surface, and the pre-printed frame having one or more wire leads;

curing the semiconductor die attached to the pre-printed frame;

forming a dam (86) to surround the recessed area to prevent a packaging material (48) from entering the recessed area;

curing the dam;

forming wire bonds (88) to couple each bond pad to

a portion of one of the wire leads that is near the recessed area;

encapsulating the wire bonds with a sealing ring (96);

curing the sealing material;

encapsulating the bottom surface of the pre-printed frame with the packaging material (48); and

curing the packaging material.

5. Method according to any of the above claims characterized in that it further comprises the step of applying a protective coating (38) over the one or more sensors of the semiconductor.

6. Method according to any of the above claims characterized in that it further comprises:

attaching a cap (68, 90) having a second opening larger than the sensors of the semiconductor die, the cap being attached to the top surface of the die carrier; and

substantially encapsulating the cap with the packaging material.

7. Semiconductor die package characterized in that it comprises:

a semiconductor die (20) having one or more bond pads on a top surface for providing terminals to one or more sensors (22), in particular optical sensors, within the top surface;

a die carrier (32) which does not extend in front of said sensors and which has one or more bond pads comprising bond terminals and having external lead bonds, the bond pads of said die carrier and the bond pads of said die determining between them an annular interface area (40) and being coupled in this area;

a sealing ring (44, 96) encapsulating said interface area (40); and

a packaging material (48) encapsulating the bottom surface of the die carrier and a bottom surface of the

semiconductor die.

8. Package according to claim 7 characterized in that it comprises:

a die carrier (32) having a first opening (34) larger than the one or more sensors but smaller than the semiconductor die and one or more external terminals; the top surface of the semiconductor die attached to the bottom surface of the die carrier such that the one or more sensors are disposed below the first opening and an interface area (40) is formed where the top surface of the semiconductor die extends beyond the first opening in the die carrier and each bond pad is coupled to a portion of one of the external terminals that is exposed on the bottom surface of the die carrier;

a sealing ring (44) encapsulating the interface area (40);

a packaging material (48) encapsulating the bottom surface of the die carrier and a bottom surface of the semiconductor die.

9. Package according to claim 8 characterized in that the sealing ring comprises a first external sealing ring (44) and a second internal sealing ring (46).

10. Package according to either of claims 8 and 9 characterized in that each bond pad is coupled to one of the external pads on the bottom surface of the die carrier by a solder bump (42).

11. Package according to any of claims 8 to 10 characterized in that the die carrier comprises a substrate and each external terminal comprises a bond pad (36) formed on a top surface of the substrate.

12. Package according to any of claims 7 to 10 characterized on that the die carrier has a pre-printed frame (60) and each external terminal comprises a wire lead (74).

13. Package according to claim 7 characterized in

that it comprises:

a pre-printed frame (80) having a recessed area (82) which is larger than the semiconductor die and one or more wire leads, a bottom surface of the semiconductor die being attached to a top surface of the recessed area of the pre-printed frame;

a wire bond (88) coupling each bond pad to a portion of one of the external terminals near the recessed area;

a dam (86) surrounding the recessed area to prevent packaging material (48) from entering the recessed area;

a sealing material (96) encapsulating each wire bond; and

a package material (48) encapsulating the bottom surface of the pre-printed frame.

14. Package according to either of claims 12 and 13 characterized in that it further comprises a cap (68, 90) having a second opening similar in size to the first opening, the cap being attached to the top surface of the pre-printed wire frame and the packaging material substantially encapsulating said cap.

15. Package according to any of claims 8 to 14 characterized in that said sealing ring and/or said packaging material comprise a thixotropic epoxy-based material.

16. Package according to any of claims 8 to 15 characterized in that the one or more sensors are covered with a protective layer (38).

17. Package according to any of claims 8 to 16 characterized in that it furthermore comprises a transparent encapsulation material in the first opening and on the top surface of the semiconductor die.

18. Package according to any of claims 8 to 17 characterized in that it furthermore comprises a lens disposed above the one or more sensors.

19. Package according to claim 14 characterized in that the cover is attached to the pre-printed frame by a polymide adhesive.

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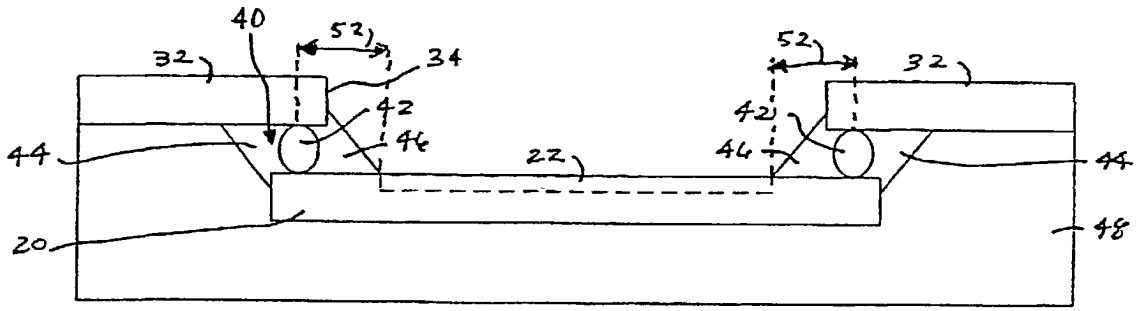
(81) États désignés *(national)*: JP, US.

[Suite sur la page suivante]

(54) Title: METHOD FOR PACKAGING A SEMICONDUCTOR CHIP CONTAINING SENSORS AND RESULTING PACKAGE

(54) Titre: PROCEDE DE MISE EN BOITIER D'UNE PUCE DE SEMI-CONDUCTEUR CONTENANT DES CAPTEURS ET BOITIER OBTENU



(57) Abstract: The invention concerns a method for producing a package (30) for a semiconductor chip comprising a semiconductor chip (20) comprising one or several bond pads on the top surface for providing terminals for one or several sensors (22) in the upper surface and a chip carrier (32) comprising an opening (34) and one or several external terminals. The semiconductor chip (20) upper surface is fixed to the chip carrier (32) lower surface such that the sensor(s) (22) are arranged beneath the first opening (34) and an interface zone (40) is formed, wherein the semiconductor chip (20) upper surface extends beyond the first opening (34) in the chip carrier (32) and each bond pad is coupled to a portion of the external terminals exposed at the chip carrier (32) lower surface for example with weld points (42). A sealing ring (44, 46) encapsulates the interface zone (40) and a coating material (48) encapsulates the chip carrier (32) lower surface and a lower surface of the semiconductor chip (20).

(57) Abrégé: Le procédé produit un boîtier (30) pour puce de semi-conducteur comprenant une puce de semi-conducteur (20) présentant une ou plusieurs plages de connexion sur une surface supérieure en vue de procurer des bornes à un ou plusieurs capteurs (22) dans la surface supérieure et un porte-puce (32) présentant une ouverture (34) et une ou plusieurs bornes extérieures. La surface supérieure de la puce de semi-conducteur (20) est fixée à la surface inférieure du porte-puce (32) de telle sorte que le ou les capteurs (22) soient disposés sous la première ouverture (34) et qu'une zone d'interface (40) soit formée, dans laquelle la surface supérieure de la puce de semi-conducteur (20) se prolonge au-delà de la première ouverture (34) dans le porte-puce (32) et que chaque plage de connexion soit couplée à une portion d'une des bornes extérieures exposée sur la surface inférieure du porte-puce (32) par exemple par des gouttes de soudure (42). Un anneau d'étanchéité (44, 46) encapsule la zone d'interface (40) et un matériau d'enrobage (48) encapsule la surface inférieure du porte-puce (32) et une surface inférieure de la puce de semi-conducteur (20).

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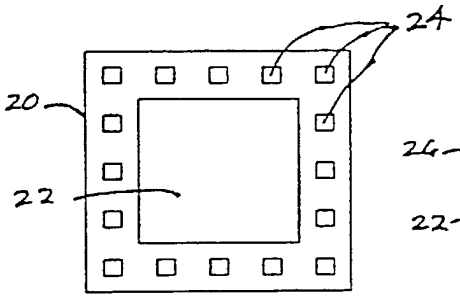

FIG. 1A

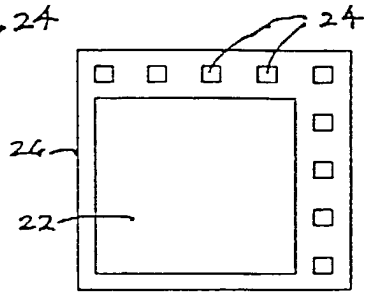

FIG. 1B

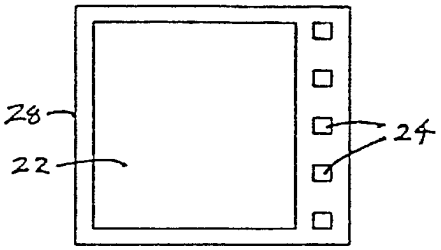

FIG. 1C

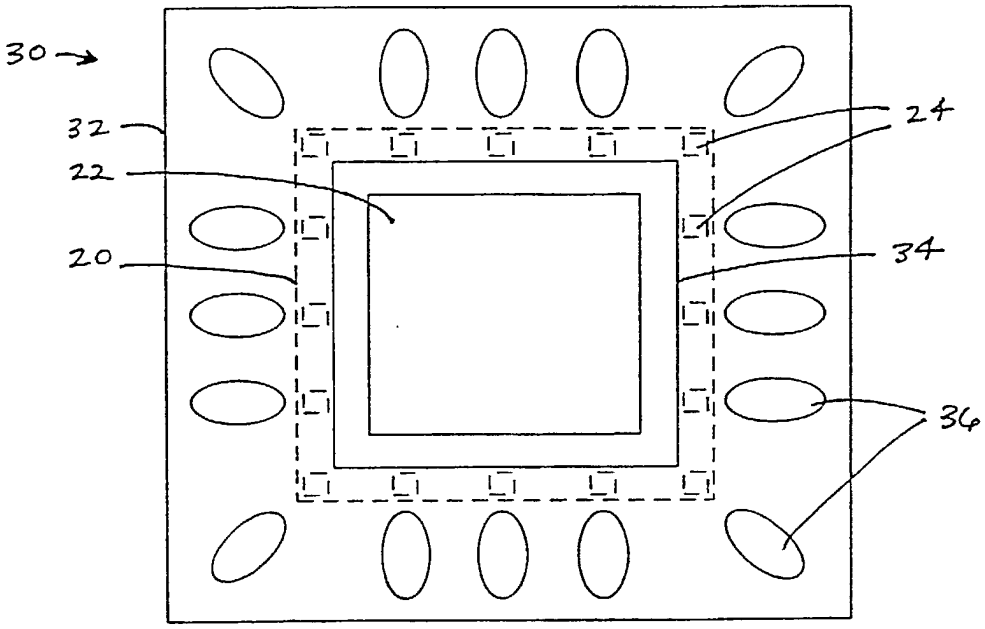

FIG. 2

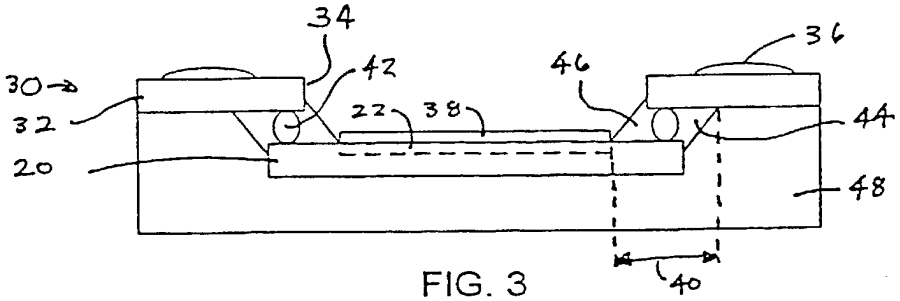

FIG. 3

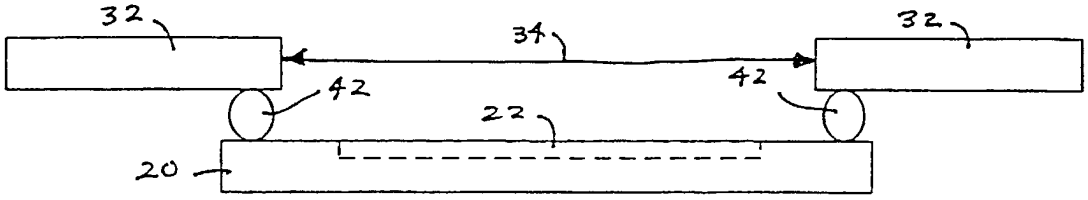

FIG. 4A

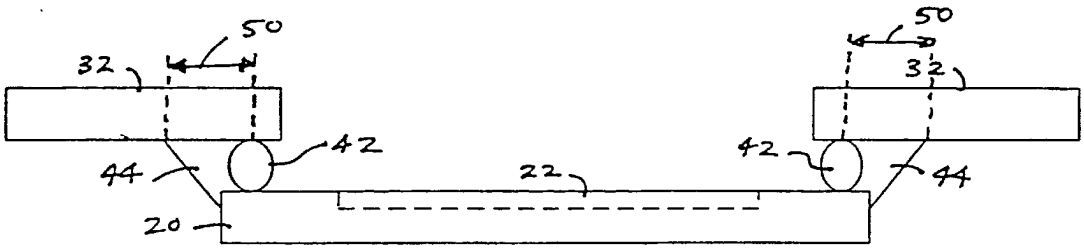

FIG. 4B

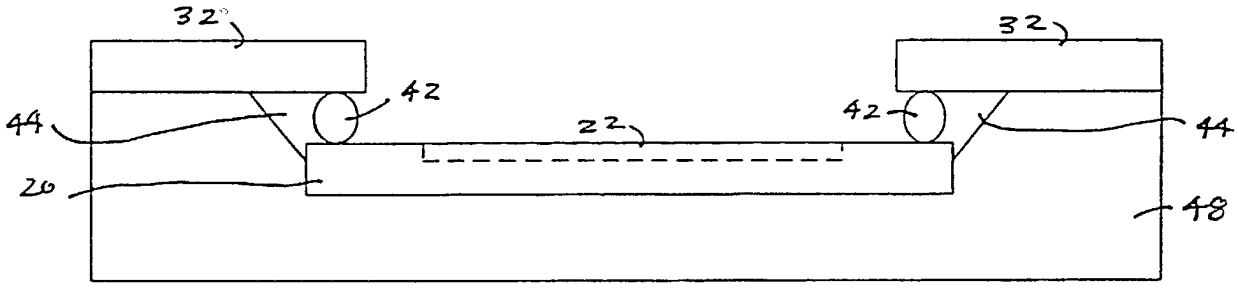

FIG. 4C

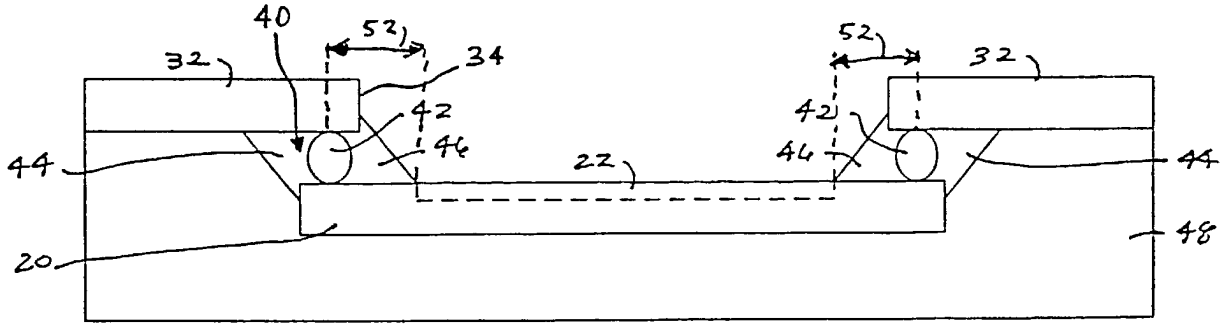

FIG. 4D

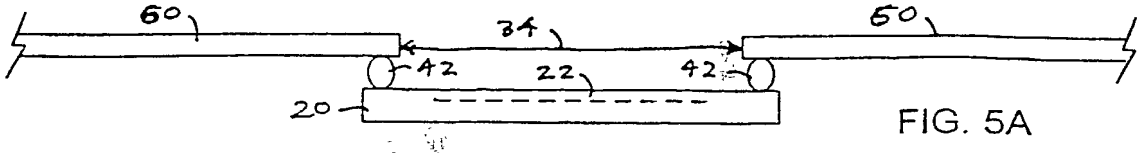

FIG. 5A

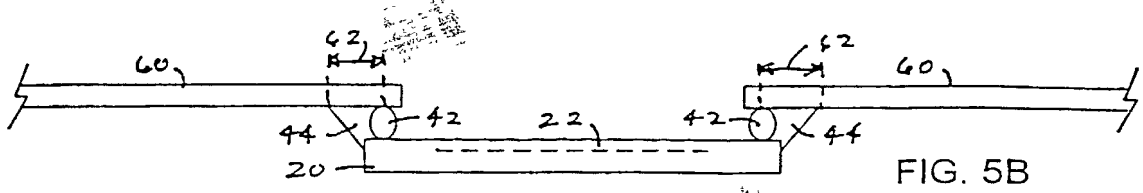

FIG. 5B

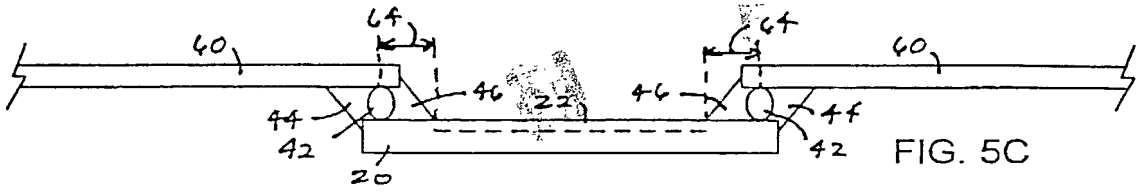

FIG. 5C

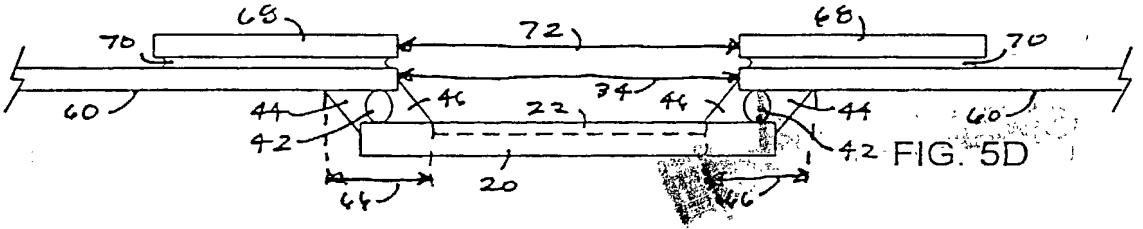

FIG. 5D

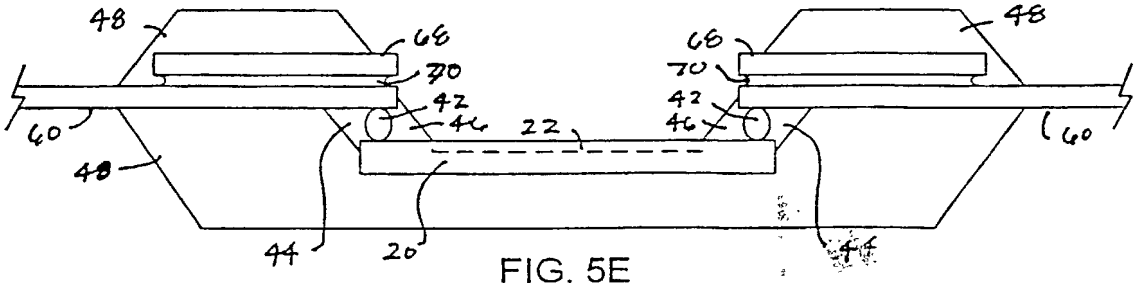

FIG. 5E

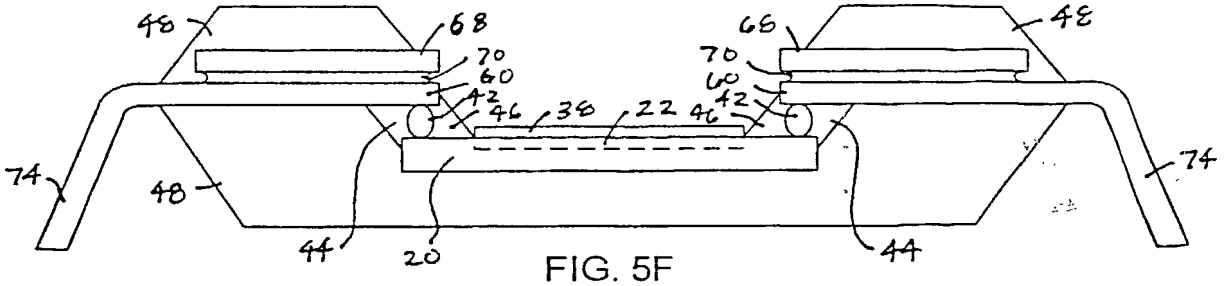

FIG. 5F

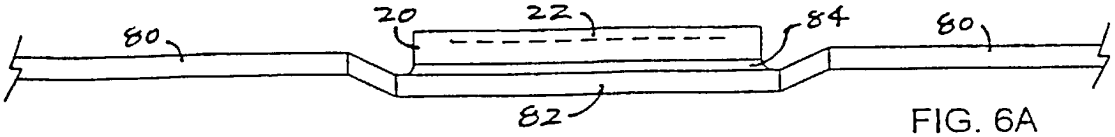

FIG. 6A

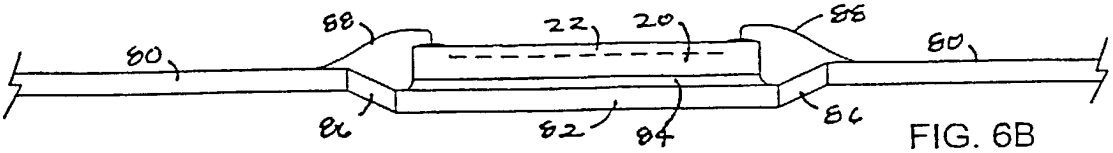

FIG. 6B

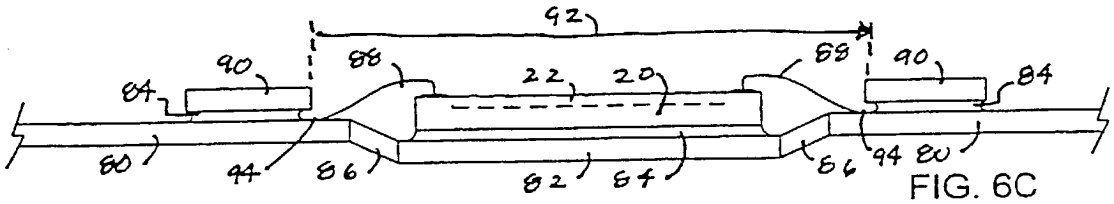

FIG. 6C

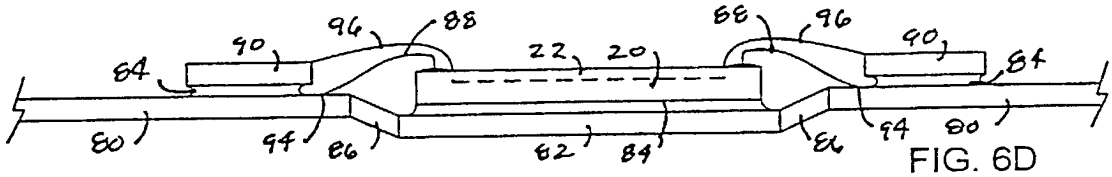

FIG. 6D

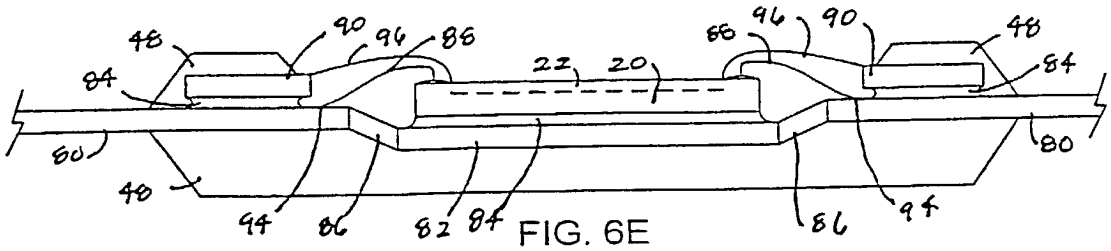

FIG. 6E

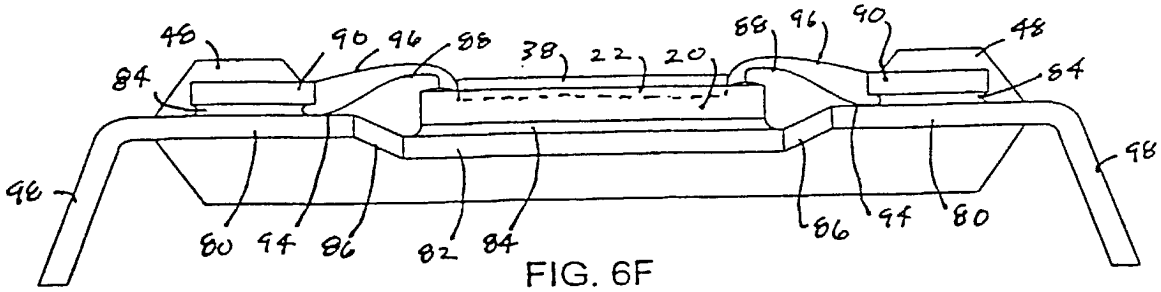

FIG. 6F

PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR PACKAGING A SEMICONDUCTOR CHIP CONTAINING SENSORS AND RESULTING PACKAGE

the specification of which: (check one)

___ is attached hereto.

XXX was filed on March 1, 2002 (international filing date of August 24, 2000)
under Attorney's Docket Number 97-GR2-144
as Application Serial No. 10/070,080
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR 1.56.

I hereby claim the benefit of foreign priority under 35 USC 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application the priority of which is claimed:

Prior Foreign Application(s):			Priority Claimed
99/11024 (Number)	FRANCE (Country)	September 2, 1999 (Filing Date)	X Yes ___ No
PCT/FR00/02367 (Number)	PCT (Country)	August 24, 2000 (Filing Date)	X Yes ___ No

I hereby claim the benefit of United States priority under 35 USC 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in a listed prior United States application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information material to the patentability of this application as defined in 37 CFR 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial #)	(Filing Date)	(Status)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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